^{60}Co γ-ray irradiation experiments and electrical modeling of TSVs in 3D ICs*

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Three-dimensional (3D) integration using through-silicon vias (TSVs) has emerged as a critical technology for extending Moore's Law as transistor scaling approaches physical limits. However, ensuring the electrical reliability of TSVs in radiation environments remains a significant challenge. This study investigates the impact of total ionizing dose (TID) irradiation on TSV transport performance and parasitic electrical parameters. Three types of test samples with varying sizes and TSV arrangements were fabricated and subjected to ^{60}Co γ-ray irradiation to measure S-parameters across different doses. A TID-dependent equivalent circuit model was developed and optimized using the Advanced Design System (ADS) to quantify the impact of TID on electrical parameters and material properties. Experimental results reveal that increasing irradiation doses lead to higher insertion loss, narrower -1 dB bandwidths, and greater group delay. Additionally, TID compresses the frequency response distribution dependent on design parameters, shifting S-parameter variations to lower frequencies. These effects are attributed to TID-induced changes in the silicon substrate, filler material, and oxide layer. The findings provide valuable insights into TSV behavior under irradiation exposure and offer a foundation for designing radiation-hardened 3D integrated circuits (ICs) for aerospace and other high-reliability applications.

Keywords: Total ionizing dose, Through silicon via, S-parameters, Equivalent circuit model, Electrical parameters

I. INTRODUCTION

With Moore's Law nearing its limits in transistor size and wafer manufacturing [1], the demand for high-performance chips continues to grow, driven by advancements in information technology and emerging industries. In aerospace applications, these chips face critical challenges, including constrained interconnect bandwidth, integration density, and power consumption [2, 3]. Post-Moore's Law, three-dimensional (3D) integration technologies have been proposed, including active integrated circuit (IC) 3D integration, 2.5D integration using passive silicon or glass interposers, and heterogeneous chip integration [1, 4]. Among these, through silicon via (TSV) technology, a vertical interconnection method, has become pivotal for extending Moore's Law. TSVs offer significant advantages, such as reduced interconnect distances, lower power consumption, increased package density, and support for device miniaturization and multifunctionality [5, 6].

Although TSV technology provides significant advantages for high-performance chips, ensuring their electrical reliability in radiation environments remains a critical challenge. Understanding the impact of total ionizing dose (TID) on TSV behavior is crucial for advancing 3D ICs, particularly in aerospace applications requiring radiation-hardened designs [7, 8]. A TSV comprises a vertical metal interconnect (typically copper) passing through a silicon substrate, surrounded by an insulating dielectric layer (commonly SiO_2) to prevent copper ion diffusion into silicon. This configuration forms a metal-oxide-semiconductor (MOS) structure, which is highly sensitive to ionizing radiation, necessitating rigorous evaluation for aerospace applications [9–12].

Multiple studies on the TID effect in MOS structures have shown that γ-ray irradiation induces charge trapping and accumulation in the oxide layer, resulting in leakage currents [13–16]. These leakage currents, along with MOS capacitance changes, contribute to signal delays and power losses in TSVs. Zeng et al. demonstrated that positive charges trapped in the oxide layer increase leakage currents and reduce the coupling capacitance in TSV arrays [17, 18]. Tian et al. examined the affects of high-energy heavy ion irradiation on TSVs, simulating the electrical performance of silicon dielectric layers subjected to varying ion energies [19]. Li et al. predicted that TSV processes alter the charge trapping behavior in the gate oxide layer, though experimental results indicated minimal impact [20]. Combined experimental and simulation approaches revealed a dose-dependent leftward shift in capacitance-vlotage (C-V) curves after irradiation [21, 22], correlating with degraded TSV performance, particularly a decline in the S_{21} parameter. Yang et al. developed a one-dimensional (1D) model using finite element analysis in COMSOL Multiphysics to further explore TID effects on TSVs [23]. Their simulations, validated by component design and irradiation experiments, revealed nonlinear TID effects on TSV devices. Specifically, the S_{21} parameter worsened with increasing irradiation dose, although the magnitude of S_{21} variation diminished at higher doses.

Focusing on the dielectric loss of SiO_2/Si heterostructures, Ref. [24] investigates the impact of TID irradiation on the alternating current (AC) characteristics of TSVs. The study found that irradiation induced a dielectric loss peak in TSVs, which shifted to lower frequencies with increasing irradiation doses. Using the Maxwell-Wagner interfacial relaxation model, the study attributes this loss to the formation of bound-

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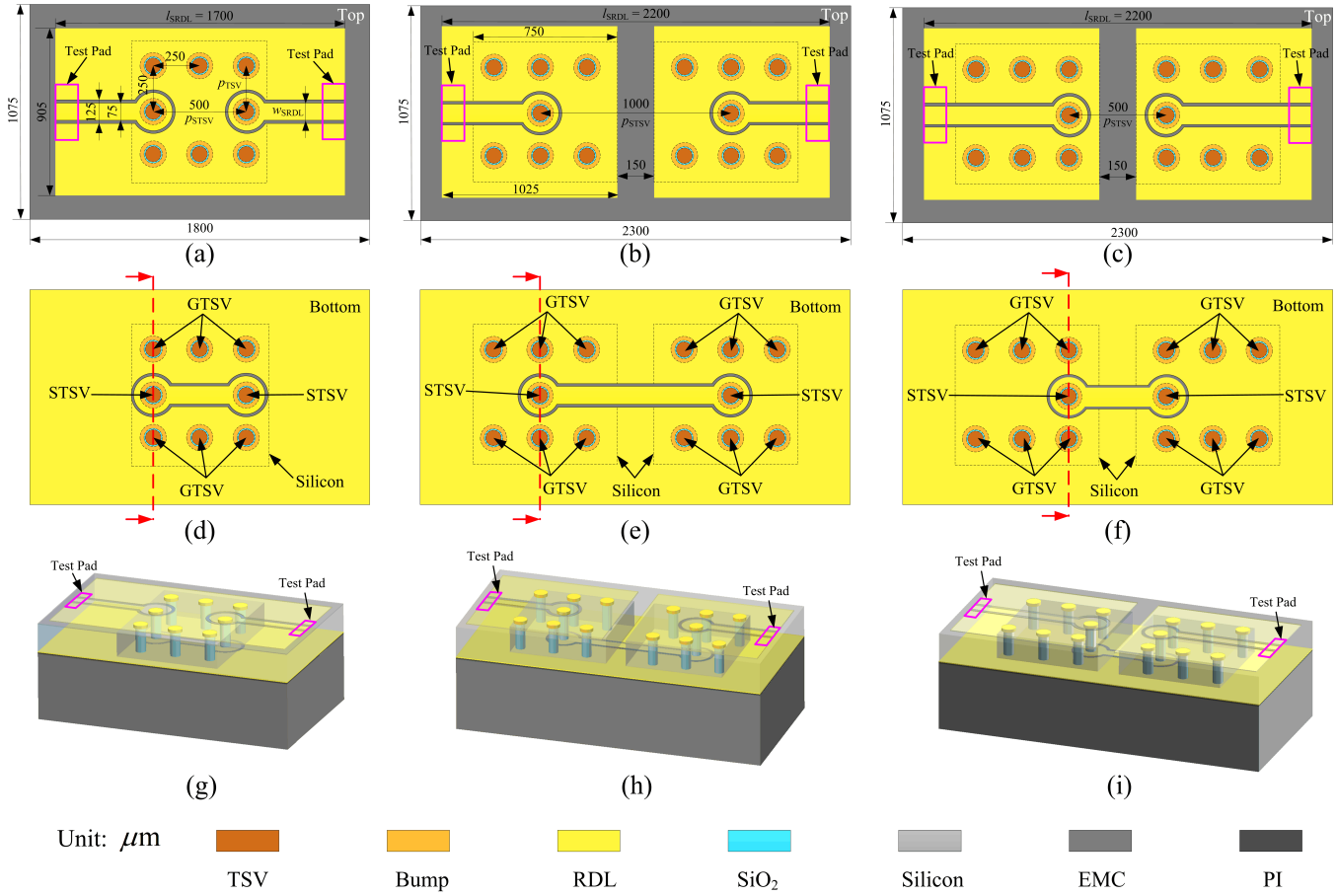

Fig. 1. (a) Top-view of sample A, (b) top-view of sample B, (c) top-view of sample C, (d) bottom-view of sample A, (e) bottom-view of sample B, (f) bottom-view of sample C, (g) 3D view of sample A, (h) 3D view of sample B, and (i) 3D view of sample C. These 3D views show the signal pathways of the TSV sample. The bottom EMC is used to support the sample. The objects are not drawn to scale.

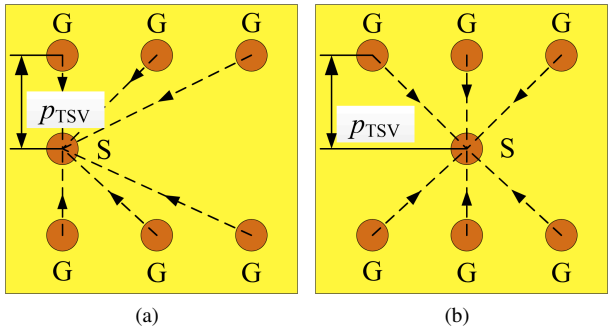

Fig. 2. Distribution of STSV with surrounding GTSVs: (a) Sample A and C and (b) Sample B. These distributions are used to calculate $p_{\mathrm{TSV\_Total}}$.

ary oxide traps (BTs). Similarly, Ref. [25] reported that ^{60}Co γ-ray irradiation on dual-channel and array TSV test chips led to a reduction in parasitic MOS capacitance and signal transmission efficiency at higher doses. The analysis revealed that TID-induced oxide and interface state trap charges lower the flat-band voltage, resulting in impedance discontinuities and signal integrity (SI) issues. These findings highlight the importance of developing predictive models to account for the degradative effects of TID on signal quality.

Existing studies on TID effects in TSVs have primarily focused on direct current (DC) leakage current and the voltage (I-V) and C-V characteristics, AC behavior, and scattering parameters. While these studies provide valuable insights, critical aspects such as the relationship between frequency response, group delay, and design parameters under TID remain underexplored. Furthermore, the interplay between parasitic electrical parameters and material properties under TID has not been fully investigated.

This paper addresses these gaps by quantifying the impact of TID on parasitic electrical parameters and material properties in TSV channels. Additionally, a predictive S-parameter model is developed to relate TSV design parameters to TID-induced material property changes. The findings contribute to the development of more reliable and radiation-hardened 3D ICs, particularly for aerospace applications. The manuscript is organized as follows: Sec. II describes the design of three types of TSV samples with bumps and redistribution layers (RDLs), along with the conditions for the ^{60}Co γ-ray irradiation experiment. In Sec. III, the scattering parameters, -1

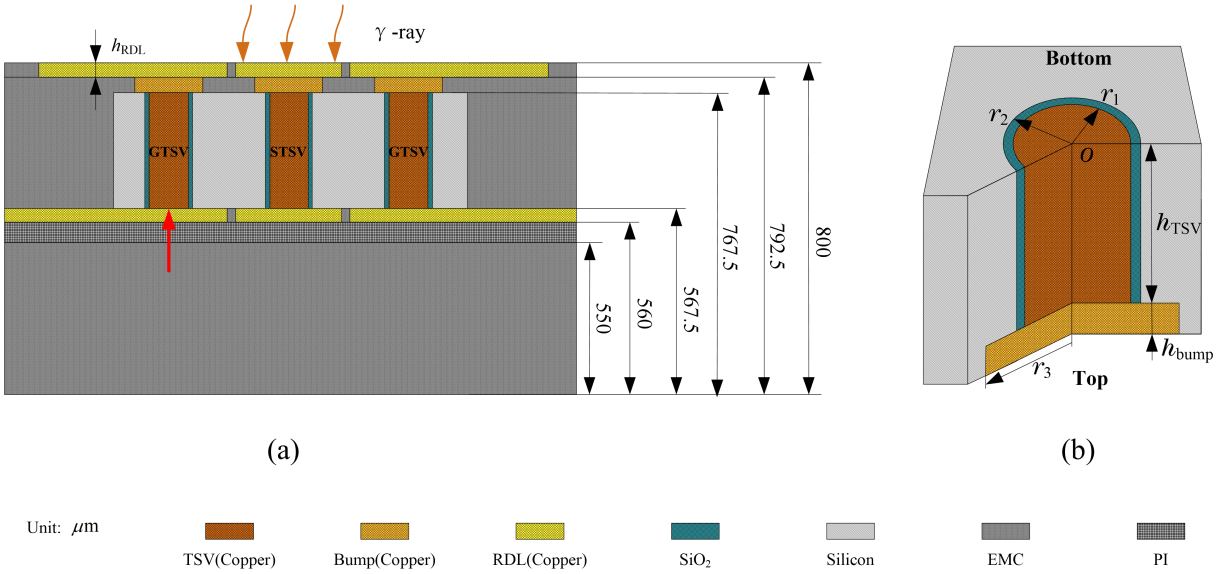

Fig. 3. (a) Cross-section view along the red dashed line of Figs. 1(d)-(f) and (b) Bottom view of a single TSV in Fig. 2(a). The objects are not drawn to scale.

TABLE 1. Design parameters of TSV samples.

Sample	Fixed parameters (μm)							Variable parameters (μm)			
	r_1	r_2	r_3	h_{TSV}	h_{Bump}	w_{SRDL}	h_{RDL}	p_{STSV}	$p_{\mathrm{TSV\_Total}}$	l_{SRDL}	FMSS
sample A								500	$2(1+\sqrt{2}+\sqrt{5})p_{\mathrm{TSV}}$	1700	Silicon
sample B	35	35.5	50	200	25	75	7.5	1000	$2(1+2\sqrt{2})p_{\mathrm{TSV}}$	2200	Silicon + EMC
sample C								500	$2(1+\sqrt{2}+\sqrt{5})p_{\mathrm{TSV}}$	2200	Silicon + EMC

dB bandwidths, frequency responses dependent on design parameters, and group delays are analyzed based on experimental results under γ-ray irradiation. Sec. IV presents the equivalent circuit model for the TSV channel. Using the validated model, the TID-dependent parasitic parameters are extracted, and the influence of the TID effect on material properties is quantified. This leads to the development of an S-parameter prediction model for the TID effect in relation to TSV design parameters and material properties. The paper concludes in Sec. V.

II. TSV SAMPLE DESIGN AND EXPERIMENTS SETUPS

Heterogeneous integration in 3D ICs combines vertical interconnections (bumps) with horizontal routing (RDLs). A comprehensive analysis of TSVs must therefore consider both the TSVs and their interactions with these components, as they are critical for signal transmission and overall system performance.

A. TSV Sample Design

Three types of TSV samples with varying bump and RDL sizes and layouts were designed. Top and bottom views of the samples are shown in Figs. 1(a) – (f). Sample A measures 1800 $\times$ 1075 μm and includes six GTSVs, while Samples B and C share identical dimensions (2300 $\times$ 1075 μm) and include twelve GTSVs each. Their 3D views are illustrated in Figs. 1(g) – (i).

Measuring TSV S-parameters on a bare wafer is challenging due to the TSV ports being located at opposite ends of the wafer. To address this, ground RDLs (GRDLs) connect the top and bottom ports of all grounded TSVs (GTSVs) to ensure consistent grounding across the array. Similarly, signal RDLs (SRDLs) link the bottom ports of signal TSVs (STSVs), enabling signal transmission between two STSVs through their respective bumps.

Although all three types of TSV samples feature the same number of GTSVs surrounding a single STSV, their arrangements differ. The shielding effect provided by the GTSVs is influenced by the pitch between the GTSV and the STSV [26–28]. This total pitch, denoted as $p_{\mathrm{TSV\_Total}}$, quantifies the shielding effect. According to the schematic in Fig. 2, $p_{\mathrm{TSV\_Total}}$ is calculated as $2(1+\sqrt{2}+\sqrt{5})p_{\mathrm{TSV}}$ for samples A and C, and $2(1+2\sqrt{2})p_{\mathrm{TSV}}$ for sample B.

The cross-section along the red dashed lines in Figs. 1(d) – (f) is shown in Fig. 3(a), while Fig. 3(b) illustrates the bottom view of a single TSV embedded in a silicon substrate. In this diagram, r_1 represents the TSV radius, r_2 the oxide layer radius, r_3 the bump radius, h_{TSV} the TSV height, and

h_{bump} the bump height. These parameters were predefined as fixed design elements in this study. Variable parameters were also introduced to enable controlled analyses and to explain variations in the experimental results.

As shown in Fig. 1, samples A and C share the same STSV pitch (p_{STSV}) but differ in their SRDL lengths (l_{SRDL}). Conversely, samples B and C have the same SRDL length but differ in p_{STSV}. Consequently, $p_{\mathrm{TSV\_Total}}$, p_{STSV}, and l_{SRDL} were defined as variable parameters. In addition, in sample A, the two STSVs are located on the same silicon substrate, where the filler material between the STSVs (FMSS) is silicon. In contrast, in samples B and C, the STSVs are on separate silicon substrates, with an epoxy molding compound (EMC) layer providing isolation. A summary of the design parameters is presented in Table 1.

B. TID Experiments Setups

Irradiation experiments were performed using a ^{60}Co γ-ray source at the Northwest Institute of Nuclear Technology, with a dose rate of 50 rad(Si)/s. Dose levels were set at 60, 120, and 180 krad(Si). All TSV samples were irradiated without any applied bias. A total of 27 samples were prepared, with nine allocated to each of the three TSV types (labeled A1#–A9#, B1#–B9#, and C1#–C9#). For each TSV type, three samples were irradiated at each dose level. A summary of the experimental conditions is presented in Table 2.

TABLE 2. Experimental conditions of TID irradiation.

Conditions	Value
Radiation sources	^{60}Co
Dose rate	50 rad(Si)/s
Dose point	60 krad(Si), 120 krad(Si), 180 krad(Si)
Temperature	25°C
Measurement equipment	Microwave probe stations and vector network analyzer

Signal transmission begins at the test pad located on one side of the top SRDL and propagates to the upper surface of the first STSV. From there, it travels through the TSV to its lower surface and is transferred via the bottom SRDL to the lower surface of the second STSV. The signal then passes through the second TSV to its upper surface and continues along the top SRDL to the measurement pad on the opposite side. The upper surfaces of the two STSVs are connected to the sample edges via two top SRDLs, forming a ground-signal-ground (GSG) test pad alongside adjacent GRDLs, as shown in Figs. 1(a) - (c), (g) - (i). The SRDLs and GRDLs are separated by an EMC layer on the same plane.

Custom-designed GSG probes were used to minimize errors associated with conventional soldering and simplify measurements. A pair of 150 μm-pitch GSG probes was mounted on a probe station and connected to a vector network analyzer (VNA) via high-frequency cables. The VNA operated across a frequency range of 0.1–25 GHz with a step size of 0.1 GHz and a 50 Ω port impedance. To mitigate errors from factors such as probe pressure and positioning, S-parameters were averaged across three identical samples for each measurement.

III. EXPERIMENTAL RESULTS AND ANALYSIS

This section analyzes the SI performance of three types of TSV samples under γ-ray irradiation, highlighting the influence of design parameters and irradiation effects on key metrics such as S_{21} magnitude, -1 dB bandwidth, and group delay.

A. Variation of scattering parameters and -1 dB bandwidth under γ-ray irradiation

The insertion loss and -1 dB bandwidth of the TSV samples were evaluated, as shown in Fig. 4. The -1 dB bandwidth is defined as the frequency range up to the maximum frequency at which insertion loss increases by 1 dB relative to the DC level.

Figs. 4(a) - 4(c) illustrate the S_{21} magnitudes for samples A, B, and C at irradiation doses of 60, 120, and 180 krad(Si). Across the 0.1–25 GHz frequency range, S_{21} magnitude initially decreases before increasing. Sample A exhibits a minimum S_{21} of -2.32 dB at 16.7 GHz, sample B reaches -2.31 dB at 13.7 GHz, and sample C shows -1.72 dB at 11.9 GHz. The lowest S_{21} values occur at the highest dose (180 krad(Si)) for all samples, with overall S_{21} magnitudes decreasing as the irradiation dose increases.

In terms of relative change, sample A shows the largest variation in S_{21} magnitude, decreasing by 0.4 dB at 16.7 GHz as the dose increases from 0 to 180 krad(Si). In contrast, sample B exhibits a smaller reduction of 0.11 dB at 13.7 GHz, while sample C shows a moderate decrease of 0.19 dB at 11.9 GHz. Correspondingly, signal transmission efficiency drops by 20.7%, 5.4%, and 12.6% for samples A, B, and C, respectively.

At 15 GHz, sample A ($p_{\mathrm{STSV}} = 500$ μm) exhibits S_{21} magnitudes of -1.87, -2.06, -2.19, and -2.27 dB for doses of 0, 60, 120, and 180 krad(Si), respectively. By contrast, sample C, with a similar p_{STSV} but different filler material, achieves higher S_{21} magnitudes (-1.58 to -1.70 dB across the same dose range). Despite sample A's shorter l_{SRDL}, which typically reduces insertion loss [29, 30], its use of silicon as the FMSS increases crosstalk, degrading signal performance compared to sample C, which uses a combination of EMC and silicon for better isolation.

The shielding effect provided by the GTSVs depends on $p_{\mathrm{TSV\_Total}}$, calculated as $2(1+\sqrt{2}+\sqrt{5})p_{\mathrm{TSV}}$ for samples A and C, and $2(1+2\sqrt{2})p_{\mathrm{TSV}}$ for sample B (Table 1). A smaller $p_{\mathrm{TSV\_Total}}$ increases the conductance (G_{Si}) and capacitance (C_{Si}) of the silicon substrate (G_{Si} and C_{Si}, defined in Sec. IV A), leading to greater insertion loss [29]. Sample B, despite its larger p_{STSV} (1000 μm compared to 500 μm for sample C), exhibits higher insertion loss due to its smaller $p_{\mathrm{TSV\_Total}}$.

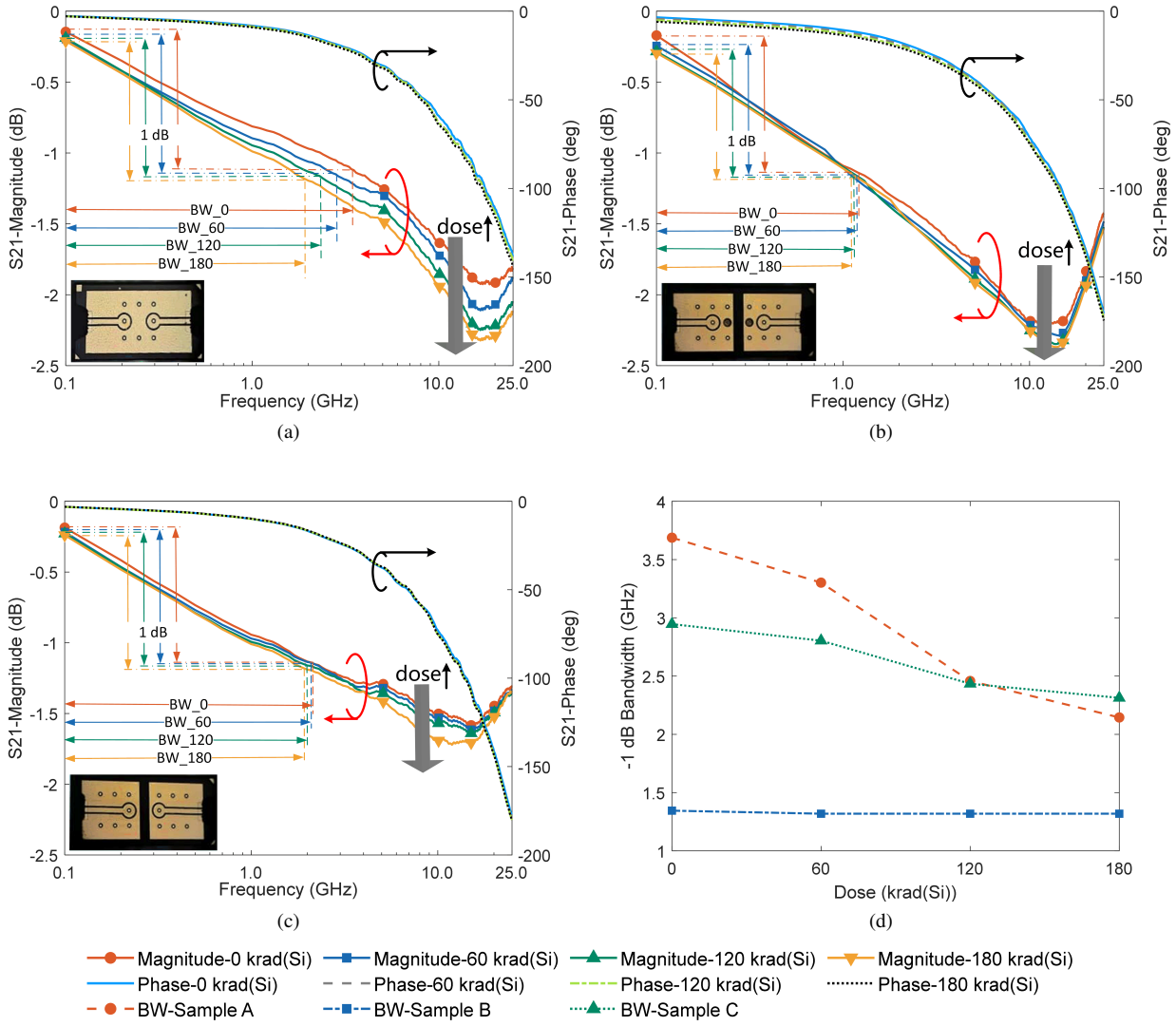

Fig. 4. S_{21} magnitude measurement results with dose variation for (a) sample A, (b) sample B, (c) sample C and (d) TID-dependent -1dB bandwidth of TSV samples.

Bandwidth analysis reveals that sample A has the largest -1 dB bandwidth before irradiation, while sample B has the smallest, as shown in Fig. 4(d). As the dose increases to 180 krad(Si), the bandwidths of samples A, B, and C decrease by 41.48%, 1.93%, and 21.49%, respectively, reflecting deteriorated suppression of inter-symbol interference (ISI). Notably, after 120 krad(Si), sample C's bandwidth surpasses that of sample A, demonstrating better ISI suppression at higher doses.

B. Variation of frequency response of design parameters-related under γ-ray irradiation

To evaluate how design parameters influence frequency response, we analyzed the impact of p_{STSV}, $p_{\mathrm{TSV\_Total}}$, l_{SRDL}, and the filler material's conductivity (σ_{Fill}) under varying TID doses. Fig. 5 illustrates the S-parameter frequency response, while Fig. 6 highlights the intersection points of S_{21} magnitudes, dividing the frequency range into three bands: low (P1), mid (P2), and high (P3). Increasing irradiation doses compress the frequency response distribution, shifting intersection frequencies from 6.2 GHz and 19 GHz at 0 krad(Si) to 1.8 GHz and 15.7 GHz at 180 krad(Si).

Despite identical p_{STSV} and $p_{\mathrm{TSV\_Total}}$ values for samples A and C, sample A is expected to exhibit lower insertion loss due to its shorter l_{SRDL}. However, significant crosstalk arises from the integration of STSVs within a single silicon substrate and the use of silicon as the FMSS in sample A. Consequently, sample A demonstrates lower S_{21} magnitudes than sample C in the P2 and P3 bands, where σ_{Fill} becomes the dominant factor affecting S_{21}.

When compared to sample B, sample A has a larger $p_{\mathrm{TSV\_Total}}$, which theoretically reduces leakage along the sil-

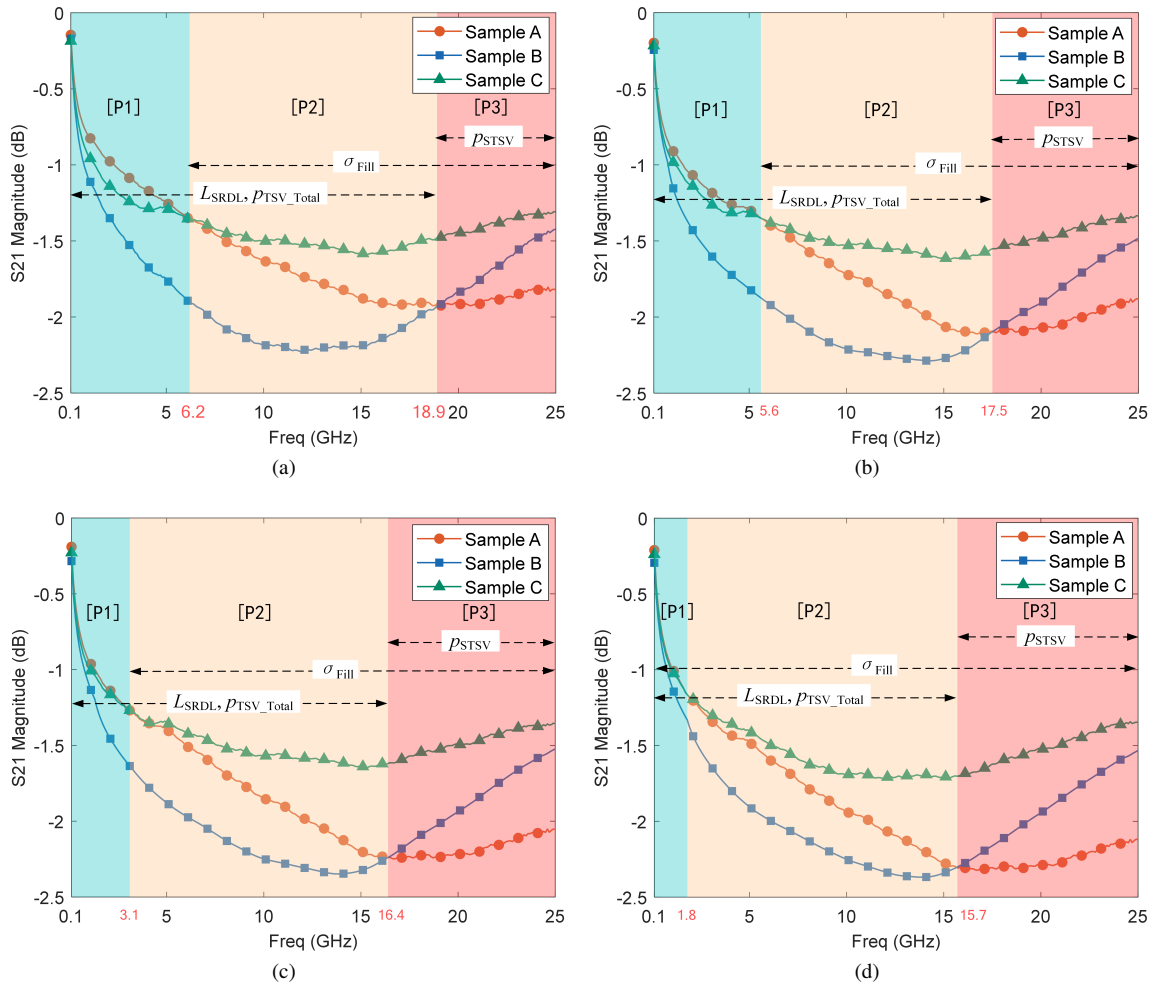

Fig. 5. Frequency response related to design factors of TSV samples at (a) 0 krad(Si); (b) 60 krad(Si); (c) 120 krad(Si) and (d) 180 krad(Si).

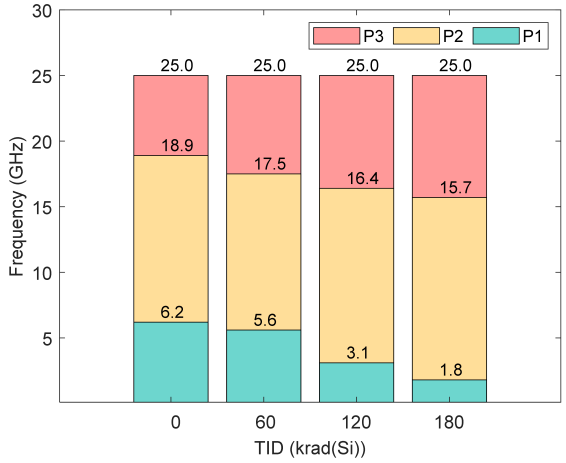

Fig. 6. TID-Induced frequency response compression in TSV samples: With increasing dose, P1, P2 and P3 boundaries shift to lower frequencies.

icon substrate and improves the S_{21} magnitude. However, the smaller p_{STSV} and the use of silicon as the FMSS in sample A lead to significant crosstalk, resulting in lower S_{21} magnitudes than those of sample B in the P3 band. Here, p_{STSV} is the primary factor influencing the S_{21} magnitude.

In the P1 and P2 bands, sample A, with its shorter l_{SRDL} and larger $p_{\mathrm{TSV\_Total}}$ compared to sample B, is expected to exhibit higher S_{21} magnitudes, as corroborated by the experimental data in Fig. 5. For samples B and C, although sample B has a larger p_{STSV}, which reduces crosstalk, its smaller $p_{\mathrm{TSV\_Total}}$ increases leakage along the silicon substrate, leading to lower S_{21} magnitudes compared to sample C. Thus, in the P1 and P2 bands, S_{21} magnitude variations are primarily influenced by the combined effects of l_{SRDL} and $p_{\mathrm{TSV\_Total}}$.

In conclusion, the variation in S_{21} magnitude across different frequency bands is primarily dictated by the design parameters. As the irradiation dose increases, these parameters progressively influence insertion loss, particularly at lower frequencies.

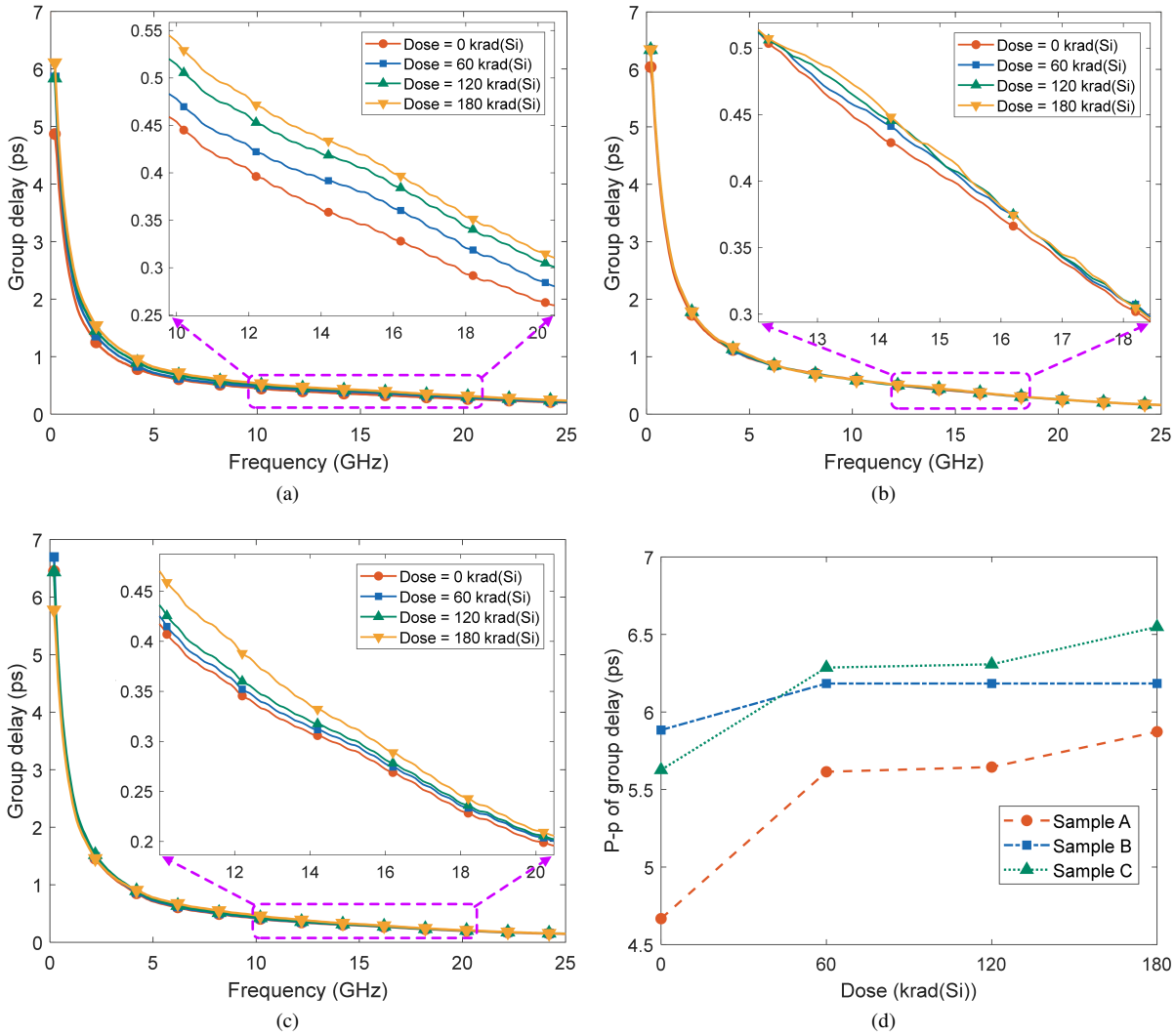

Fig. 7. Group delay with dose variation for (a) sample A, (b) sample B, (c) sample C and (d) peak to peak of group delay.

C. Variation of group delay under γ-ray irradiation

Group delay, defined as the negative derivative of phase with respect to frequency, as expressed in Eq. (1), reflects phase variations across frequencies. Figs. 7(a) – 7(c) present the group delay for all samples, showing a gradual decrease with increasing frequency (0.1–25 GHz). However, higher TID doses result in significant group delay increases at 15 GHz: 0.3466 ps to 0.4203 ps (21.26%) for sample A, 0.4049 ps to 0.4212 ps (4.03%) for sample B, and 0.2925 ps to 0.3157 ps (7.93%) for sample C.

$$\tau = -\frac{\mathrm{d}\varphi}{\mathrm{d}\,(2\pi f)} \tag{1}$$

As shown in Fig. 7(d), peak-to-peak group delay also increases with irradiation dose, indicating greater phase differences across the broadband spectrum, which exacerbate ISI and degrade SI.

IV. ELECTRICAL MODELING OF THE TSV CHANNEL

The TSV channel consists of four primary materials: copper for the TSVs, bumps, and RDLs; silicon for the substrates; silicon dioxide as a thin insulating layer surrounding the TSVs; and an epoxy molding compound (EMC) as the isolation material. TID irradiation alters the material properties, including the conductivity of copper, the conductivity and dielectric constant of the silicon substrate, and the dielectric constant of the oxide layer. To evaluate the impact of TID irradiation on TSV channel performance, a TID-dependent TSV model is required. This model must also account for additional factors, such as the significantly greater length of the RDLs compared to the height of the TSVs [29].

TABLE 3. Description of parameter symbols.

Symbol	Description	Symbol	Description
$R_{\text{RDL\_Top}}$	Resistance of top RDL	$C_{\text{RDL\_Top}}$	Capacitance of top RDL
$R_{\text{RDL\_Bot}}$	Resistance of bottom RDL	$C_{\text{RDL\_Bot}}$	Capacitance of bottom RDL
$R_{\text{Si\_RDL}}$	Resistance of top RDL to silicon substrate	C_{Fill}	Capacitance of top RDL to EMC
$L_{\text{RDL\_Top}}$	Inductance of top RDL	$L_{\text{RDL\_Bot}}$	Inductance of bottom RDL
R_{TSV}	Resistance of TSV	L_{TSV}	Inductance of Top
C_{oxs}	Capacitance of oxide layer of STSV	C_{oxg}	Capacitance of oxide layer of GTSV
R_{Si}	Resistance of silicon substrate	C_{Si}	Capacitance of silicon substrate
$R_{\text{Crosstalk}}$	Resistance of crosstalk of STSV-STSV	$C_{\text{Crosstalk}}$	Capacitance of crosstalk of STSV-STSV
C_{Bump}	Capacitance of bump		

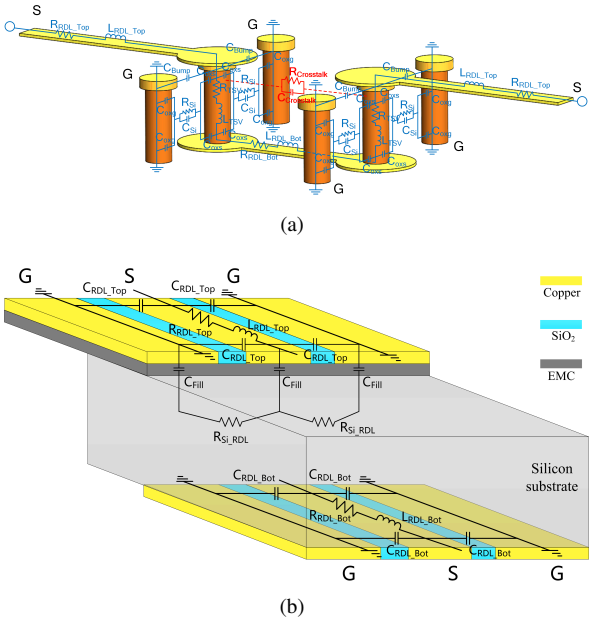

Fig. 8. GSG-type equivalent circuit model of (a) TSV channel and (b) RDL layer for conducting an optimization design in ADS to quantitatively investigate the impact of TID on the electrical parameters of the TSV channel.

A. Equivalent circuit Modeling

The TSV channel model for the three test sample types is shown in Fig. 8(a). It consists of three main components: the top RDL used for probing, the TSV structure, and the bottom RDL serving as an interconnection point. Fig. 8(b) provides a detailed representation of the RDL models at the top and bottom of the TSV. Due to the symmetrical arrangement of the RDLs, only one top-layer RDL model is shown in Fig. 8(b).

Both the RDLs and TSVs, made of copper, are represented as a series of resistances and inductances. The TSVs are coated with a thin layer of silicon dioxide, which is modeled as a capacitor. The silicon substrate is modeled as a parallel network of resistors and capacitors, while the connections between GTSVs and STSVs are represented by an RC network. Crosstalk between STSVs is accounted for using an additional RC model, highlighted by the red dashed lines in Fig. 8(a). Table 3 summarizes the electrical parameters of the TSV channel model.

Fig. 8(b) also provides a more detailed model of the RDL structure. The SRDL connects the horizontally aligned STSVs, while the GRDL connects the horizontally aligned GTSVs. These components are electrically isolated by an insulating layer, which is represented as a capacitor in the model. Additionally, the top RDL is separated from the silicon substrate by an EMC layer, which is also modeled as a capacitor. To account for the penetration of the electric field into the dielectric layers and the silicon substrate beneath the RDL, the model incorporates the effective conductivity of the silicon substrate.

The RC model for the silicon substrate is defined by Eqs. (2) and (3), where R_{sub} and C_{sub} represent the resistance and capacitance of the substrate between an STSV and the surrounding GTSVs. When mapping this model to the GSG-type equivalent circuit shown in Fig. 8(a), adjustments are made to account for the specific distribution of GTSVs around the STSV.

$$C_{\text{Sub}} = \frac{\pi \varepsilon_0 \varepsilon_{\text{Si}}}{cosh^{-1}(p_{\text{TSV}}/d_{\text{TSV}})} \times h_{\text{TSV}} \tag{2}$$

$$R_{\text{Sub}} = \frac{cosh^{-1}(p_{\text{TSV}}/d_{\text{TSV}})}{\pi \sigma_{\text{Si}} h_{\text{TSV}}} \tag{3}$$

where ε_0 is the permittivity of vacuum, ε_{Si} is the relative permittivity of silicon (11.9), σ_{Si} is the conductivity of silicon (10 S/m), p_{TSV} is the STSV-to-GTSV pitch (250 μm), and d_{TSV} is the TSV diameter.

The relationship between capacitance and conductance in the silicon substrate is expressed as Eq. (4) [29]:

$$\frac{C_{\text{Sub}}}{G_{\text{Sub}}} = \frac{\varepsilon_{\text{Si}}}{\sigma_{\text{Si}}} \tag{4}$$

The equivalent resistances and capacitances for samples A, B, and C are calculated using these equations and the $p_{\text{TSV\_Total}}$ values defined in Fig. 2. For example, the resistances for samples A and C are given by:

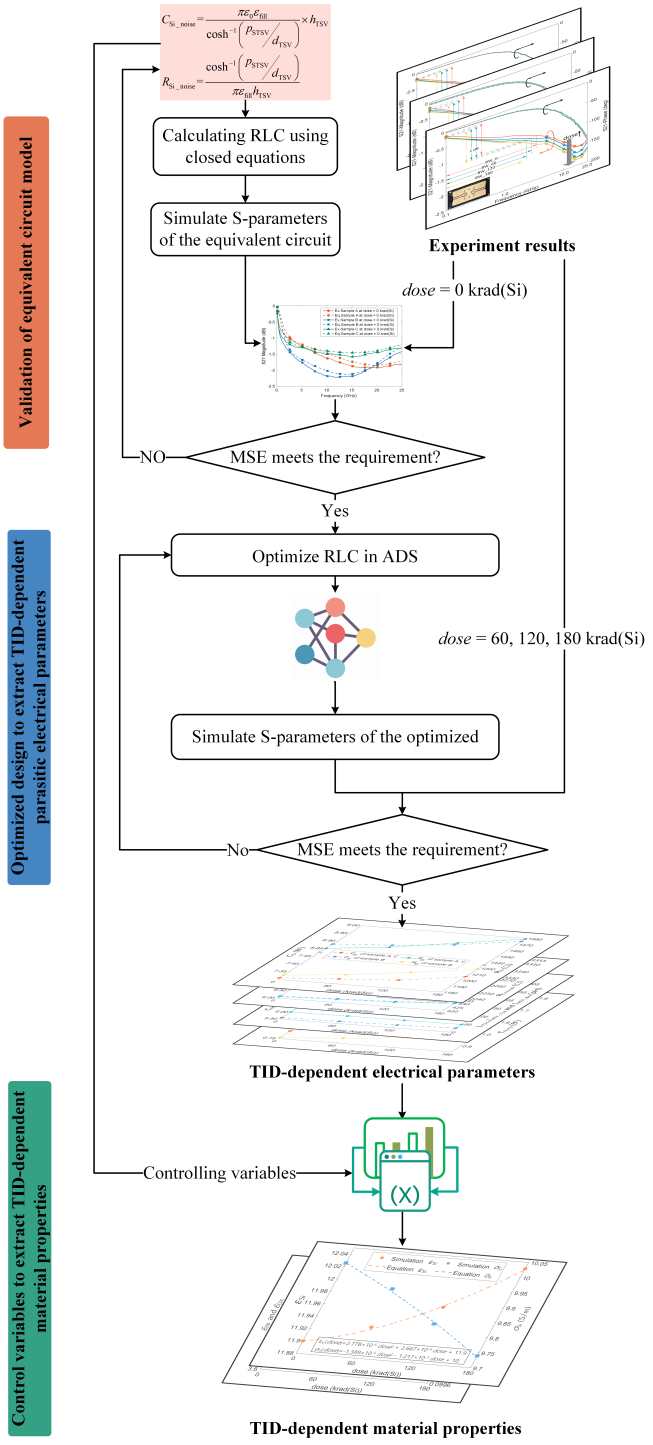

Fig. 9. Verification of the equivalent circuit model at 0 krad(Si) for the process of extracting TID dependent electrical parameters and material properties.

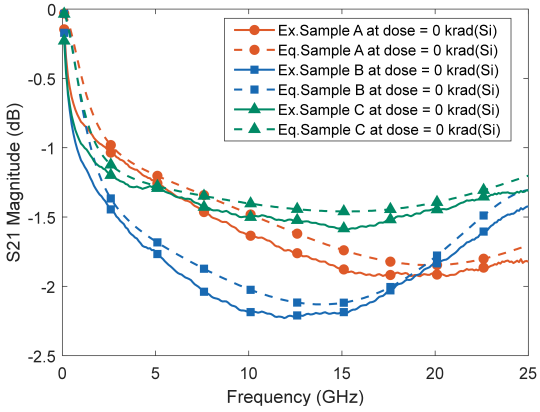

Fig. 10. Comparison of S_{21} magnitudes obtained by experiment and the equivalent circuit model. The validated TSV channel models at 0 krad(Si) are employed for extracting the electrical parameters of the equivalent circuit at doses of 60, 120, and 180 krad(Si), as well as determining the variation of material properties with dose based on the extracted electrical parameters coupled with closed-form equations.

$$R_{\mathrm{Si}}^{\mathrm{A}} = R_{\mathrm{Si}}^{\mathrm{C}} = (1+\sqrt{2}+\sqrt{5})R_{\mathrm{sub}} \tag{5}$$

with corresponding capacitances:

$$C_{\mathrm{Si}}^{\mathrm{A}} = C_{\mathrm{Si}}^{\mathrm{C}} = \frac{C_{\mathrm{sub}}}{1+\sqrt{2}+\sqrt{5}} \tag{6}$$

For sample B:

$$R_{\mathrm{Si}}^{\mathrm{B}} = (1+2\sqrt{2})R_{\mathrm{sub}} \tag{7}$$

And the C_{Si} is calculated as

$$C_{\mathrm{Si}}^{\mathrm{B}} = \frac{C_{\mathrm{sub}}}{1+2\sqrt{2}} \tag{8}$$

The crosstalk RC model between STSVs is described by Eqs. (9) and (10), where $\varepsilon_{\mathrm{fill}}$ denotes the relative permittivity of the FMSS, and σ_{fill} represents its conductivity. As illustrated in Fig. 1, for sample A, both STSVs are located within the same silicon substrate. In this configuration, $\varepsilon_{\mathrm{fill}}$ is equivalent to $\varepsilon_{\mathrm{Si}}$, and σ_{fill} is equal to σ_{Si}. Conversely, in samples B and C, the two STSVs are situated in separate silicon substrates, separated by an EMC layer. For these two samples, $\varepsilon_{\mathrm{fill}}$ (value of 3.7) is lower than $\varepsilon_{\mathrm{Si}}$, and σ_{fill} is significantly lower than σ_{Si}.

$$C_{\mathrm{Crosstalk}} = \frac{\pi\varepsilon_0\varepsilon_{\mathrm{fill}}}{cosh^{-1}(p_{\mathrm{STSV}}/d_{\mathrm{TSV}})} \times h_{\mathrm{TSV}} \tag{9}$$

$$R_{\mathrm{Crosstalk}} = \frac{cosh^{-1}(p_{\mathrm{STSV}}/d_{\mathrm{TSV}})}{\pi\sigma_{\mathrm{fill}}h_{\mathrm{TSV}}} \tag{10}$$

In GSG-type TSVs, the capacitance (C_{oxg}) of the oxide layer in the GTSV was determined through full-wave simulation and is approximately 1.5 times C_{oxs}. The value of C_{oxs} was calculated using Eq. (11) [31]. The capacitance models

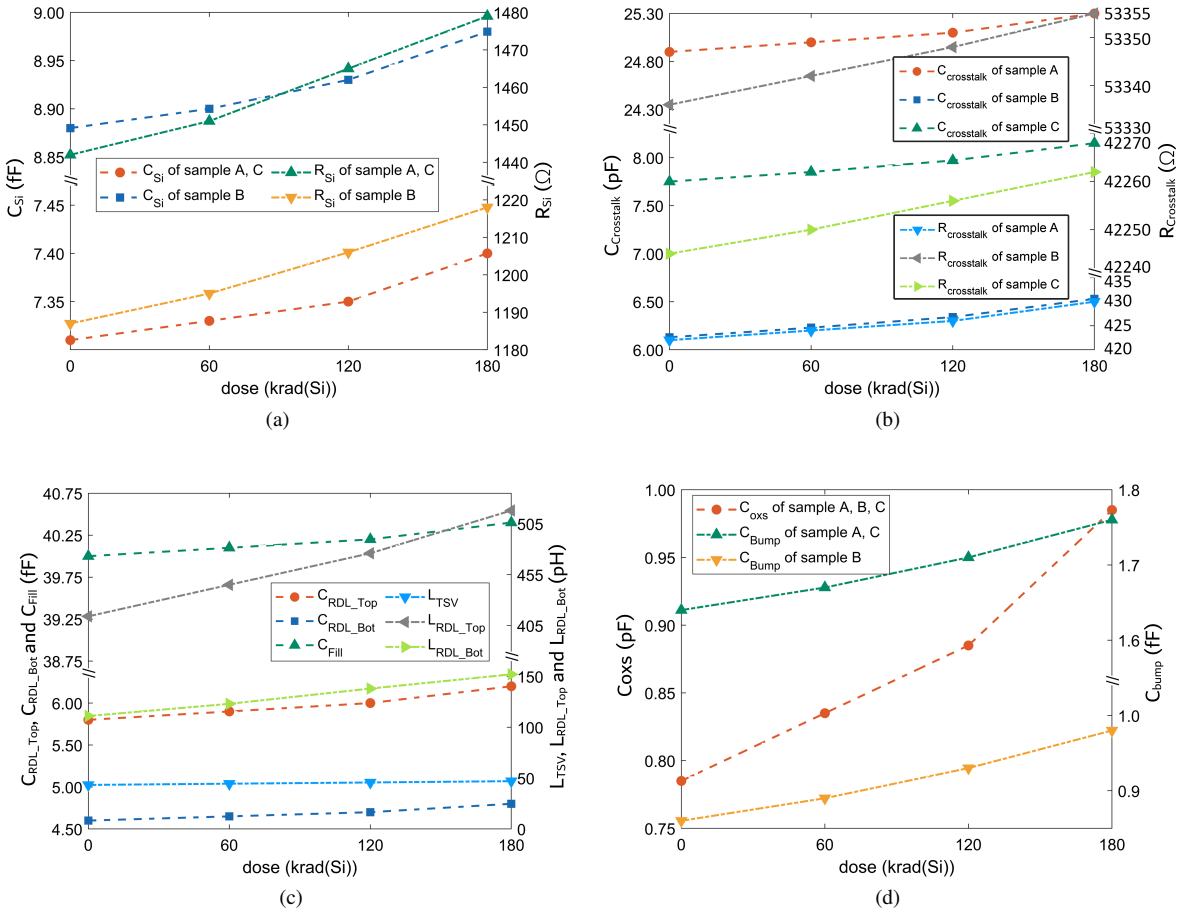

Fig. 11. Impact of TID on electrical parameters for TSV channel: (a) C_{Si} and R_{Si}, (b) $C_{\mathrm{Crosstalk}}$ and $R_{\mathrm{Crosstalk}}$, (c) $C_{\mathrm{RDL\_Top}}$, $C_{\mathrm{RDL\_Bot}}$, C_{Fill}, L_{TSV}, $L_{\mathrm{RDL\_Top}}$ and $L_{\mathrm{RDL\_Bot}}$, (d) C_{oxs}, and C_{Bump}. The electrical parameters at 0 krad(Si) are calculated by closed-form equations and those at 60, 120, 180 krad(Si) are obtained by optimization design in ADS.

for the RDL interconnects ($C_{\mathrm{RDL\_Top}}$, $C_{\mathrm{RDL\_Bot}}$, and C_{Fill}) are more complex. To compute these capacitances, the conformal mapping method is employed, which utilizes the complete elliptical integral of the first kind, as detailed in [32]. Other electrical parameters of the TSV channel were calculated based on the methodology described in [29].

$$C_{\mathrm{oxs}} = \frac{1}{2} \times \frac{\pi \varepsilon_0 \varepsilon_{\mathrm{ox}} h_{\mathrm{TSV}}}{ln((r_{\mathrm{TSV}} + t_{\mathrm{ox}})/r_{\mathrm{TSV}})} \tag{11}$$

where, $\varepsilon_{\mathrm{ox}}$ is the dielectric constant of the oxide layer and t_{ox} is the thickness of the oxide layer.

B. Extraction of TID dependent parasitic electrical parameters

At pre-irradiation (dose = 0 krad(Si)), the electrical parameters of the equivalent circuit model were calculated using closed-form equations based on device dimensions and material properties. However, as the irradiation dose increased, these parameters varied, necessitating an iterative optimization process. The equivalent circuit model shown in Fig. 8 was constructed using Advanced Design System (ADS), validated under pre-irradiation conditions, and subsequently optimized to account for TID effects. The optimization minimized the mean square error (MSE) between simulated and experimentally measured S-parameters.

Fig. 10 compares the S_{21} magnitudes obtained from experimental measurements and the equivalent circuit model. The MSE values for samples A, B, and C were 0.0177, 0.0222, and 0.0143, respectively. These low MSE values demonstrate a strong correlation between the model and experimental data, validating the accuracy of the proposed TSV channel model.

The optimized design process is illustrated in Fig. 9, which enabled the extraction of electrical parameters for individual TSV samples across various irradiation doses, as shown in Fig. 11(a). As the dose increased, both C_{Si} and R_{Si} exhibited a significant rise for all three sample types, leading to higher insertion loss. This effect is attributed to reduced impedance along the leakage path to the silicon substrate, described by $Z = R + 1/j\omega C$ [29]. Consequently, as shown in Fig. 4, insertion loss increased with dose, primarily due to the ele-

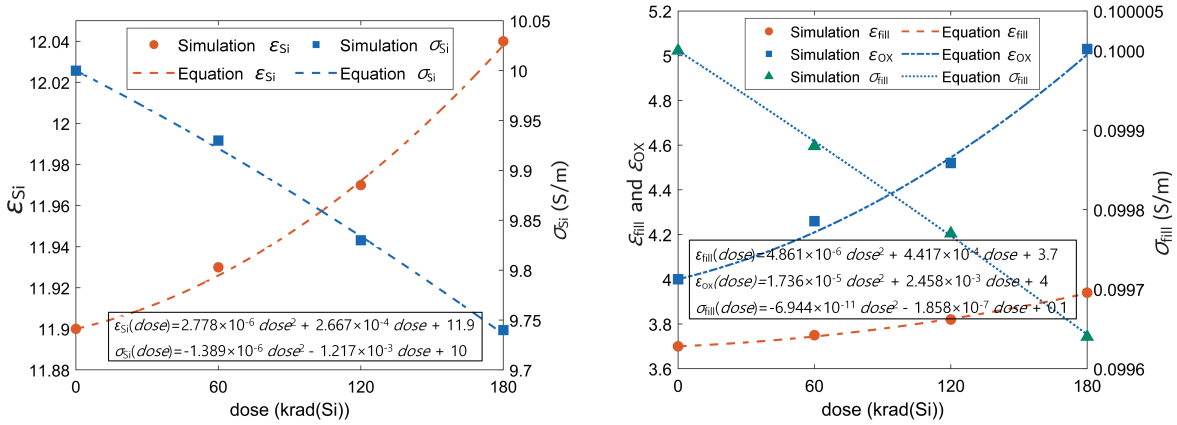

Fig. 12. TID-dependent equations for TSV material properties of (a) $\varepsilon_{\mathrm{Si}}$ and σ_{Si} (b) $\varepsilon_{\mathrm{fill}}$, $\varepsilon_{\mathrm{OX}}$ and σ_{fill}. Ignoring the variation of mechanical stresses, the TSV channel dimensions are fixed. The variation of the electrical parameters in Fig. 10 is caused by the changes in material properties (scattered dots) due to the TID radiation. The correlation equation between material properties (dashed lines, dot - dash line and double-dash line) and dose was obtained by polynomial fitting.

vated values of C_{Si} and R_{Si}. Similarly, Fig. 11(b) shows that $C_{\mathrm{Crosstalk}}$ and $R_{\mathrm{Crosstalk}}$ also increased with dose, further contributing to insertion loss via reduced impedance along the leakage path to the FMSS. Notably, the FMSS materials in samples B and C (EMC and silicon) exhibit lower conductivity compared to the silicon used in sample A, resulting in significantly higher $R_{\mathrm{Crosstalk}}$ for samples B and C.

The parameters $C_{\mathrm{RDL\_Top}}$, $C_{\mathrm{RDL\_Bot}}$, C_{Fill}, L_{TSV}, $L_{\mathrm{RDL\_Top}}$, and $L_{\mathrm{RDL\_Bot}}$ were identical across all three sample types and consistent with the methodology outlined in [29]. As the dose increased, all parameters exhibited growth, with the inductances of the top and bottom RDLs showing more pronounced changes than the other parameters, as shown in Fig. 11(c). Additionally, Fig. 11(d) shows that both C_{oxs} and C_{Bump} increased with dose. Since C_{Bump} depends on the arrangement of GTSVs surrounding the STSV (Fig. 1), samples A and C, which share the same GTSV configuration, showed identical C_{Bump} values.

C. Analysis of changes in properties of TSV materials under γ irradiation

The model validated at 0 krad(Si) in Section IV A is employed to extract the parasitic electrical parameters of the TSV channel under TID radiation, as shown in Fig. 9. Additionally, it facilitates the estimation of TID-induced effects on the material properties of TSV channels through closed-form equations.

The electrical parameters of the TSV channel include geometric parameters (such as TSV radius, height, and pitch) and material properties (such as dielectric constant and conductivity). In the absence of TID-induced mechanical stress, the geometric parameters remain constant, while only material properties are affected. Consequently, the variations in electrical parameters shown in Fig. 11 are attributed to TID-induced changes in material properties. Based on this observation, the TID-dependent material properties presented in Fig. 12 were derived following the process shown in Fig. 9, establishing a quadratic relationship between material properties and irradiation dose. This enhancement transforms the calculation of electrical parameters in the TSV model (Fig. 8) from fixed equations to dose-dependent functions, enabling the prediction of signal loss in the TSV channel at varying irradiation doses.

The proposed TSV electrical model is developed using a methodology that integrates design parameters and TID effects. This model serves two primary purposes: predicting the frequency response of TSVs under TID irradiation and generating datasets for training machine learning models, which will be a focus of our future work. To the best of our knowledge, there are no EDA simulation tools that support the modelling of TSV frequency response under TID irradiation. At this stage, the lack of TID-related data—such as DC, AC, C-V characteristics, impedance measurements, and time-domain eye diagrams—limits the model. Furthermore, the model does not incorporate electrical stress or process parameters, such as doping, which are crucial for developing a more comprehensive and accurate TSV model. Similar to Ref. [21–24], we do not apply a bias during irradiation. However, we are aware that the irradiation effect can be significantly modulated by the bias. Our future work will address these limitations by obtaining the necessary data and incorporating additional parameters to enhance the model and improve its predictive accuracy.

V. CONCLUSION

This study comprehensively analyzed the impact of TID irradiation on TSV channel. By fabricating and testing three types of TSV samples under ^{60}Co γ-ray irradiation, the re-

search demonstrated that TID significantly degrades TSV electrical performance, increasing insertion loss, narrowing -1 dB bandwidth, and elongating group delay. A TID-induced compression effect on the frequency response was also observed, shifting S-parameter changes to lower frequencies. Key design factors influencing S_{21} magnitude across different frequency bands were identified. To quantify TID-induced changes in parasitic electrical parameters and material properties, a TID-dependent equivalent circuit model was developed and validated. The model accurately predicts S-parameters and offers insights into underlying physical mechanisms, such as the alteration of conductivity and dielectric constant in silicon and oxide materials. Despite its success, the model's limitations were acknowledged, with directions for future research outlined. Overall, this study enhances the understanding of TID effects on TSVs and provides a theoretical foundation for designing reliable and radiation-hardened 3D integrated circuits. The findings are particularly relevant for aerospace applications and serve as a valuable resource for optimizing TSV designs and predicting performance in radiation-prone environments.

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